**Assignment 6**

**Assignment** All assignments are to be submitted strictly before start of next lab session through online only. Late assignments will not be entertained and will be awarded ‘0’ marks.

1. **Write the Verilog code and testbench for 4:1 Multiplexer using data flow modeling.**

**Ans: Link1:** [**https://www.edaplayground.com/x/CBJW**](https://www.edaplayground.com/x/CBJW)

***2. Satisfy yourself that below code is 1:8 demux. (hint: write the testbench for the same and check)***

**Ans: Link2:** [**https://www.edaplayground.com/x/7Gaz**](https://www.edaplayground.com/x/7Gaz)

**3. Verilog code and testbench for implementing 2-input XOR gate using 2x1 multiplexer in structural modeling.**

**Ans: Link3:** [**https://www.edaplayground.com/x/MMY5**](https://www.edaplayground.com/x/MMY5)

**Self-Practice and self-evaluation**

1. Verilog code and testbench for implementing 2-input NAND gate using 2x1 multiplexer in structural modeling.

2. Verilog code and testbench for a 4-input 4-output 1-channel communication system using 4x1 multiplexer and 1x4 demultiplexer, control the select lines of multiplexer and demultiplex to switch the channel data between 4-input lines.

3. Verilog code and testbench for 8x1 multiplexer using 4x1 multiplexer and 2x1 multiplexer in structural modeling.